REMARKS

Claims 1-30 are currently pending in the application. Claims 2-13 are withdrawn from consideration. By this amendment, claims 1, 14, 15, 24 and 26 are amended for the Examiner's consideration. The foregoing separate sheets marked as "Listing of Claims" shows all the claims in the application, with an indication of the current status of each .

In the specification, the paragraphs beginning at page 6, line 19, at page 11, line 18, at page 13, line 14 and at page 14, line 11 have been amended to correct typographical errors.

The Examiner's indication that claims 20-21 and 29 contain allowable subject matter is acknowledged with appreciation.

The Examiner maintains rejection of claims 1, 24-28 and 30 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,040,605 to Sano et al. ("Sano"), and further maintains rejection of claims 14-19 and 22-23 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,273,921 to Neudeck et al. ("Neudeck").

As described in the background section of the present invention, improved FET performance can be obtained by placing gates on multiple sides of an FET channel, provided the silicon is thin enough to be fully depleted (page 2, lines 6-8). However, the prior art fabrication schemes "have relied upon lithographically defined silicon channels and long, confined lateral epitaxial growth" (page 5, lines 24-25). Horizontal double-gated structures are difficult to fabricate because alignment of the top and bottom of the gates cannot be achieved within the desired tolerances with state of the art lithographic equipment, and because the layers between the top and bottom gates frustrate self-aligning techniques (page 2, lines 22-26). Lithographically defined gates are the simplest, but fail to achieve silicidation of thin diffusions,

Received from < > at 8/18/03 11:48:42 PM [Eastern Daylight Time]

fabrication of the wraparound gate without misalignment, and fabrication of sufficiently narrow diffusions (page 5, lines 2-14).

The invention, as summarized at page 10, lines 19-24, overcomes these difficulties and provides

> "a very thin diffusion region using a known technique for growing epitaxial regions to form the very thin channel and has the advantages of providing much tighter tolerances on channel thickness than a lithographically defined channel which can be maintained by selective etching and that epitaxial growth is not complicated by the presence of thin confining layers."

This is accomplished, as summarized at page 10, lines 13-18, by the steps of

> "forming silicon layers on a substrate. Next, epitaxial channels are formed on a side surface of the silicon layers, with one side wall of the channels therefore being exposed. The silicon layers are then removed, thereby exposing a second sidewall of the epitaxial channels. Source and drain regions are then formed, coupled to ends of the epitaxial channels. Finally, a gate is formed over the epitaxial channels."

The Sano reference is a memory device. As a careful examination of Figures 2a and 2b of Sano show, the "channels" in Sano are formed on the ends of the source and drain elements, which are unrelated by geometry and function to the thin central semiconductor region of the present invention. The terminology "both sides" as used in Sano (col 11, line 57) is misleading because it does not refer, as in the present invention, to the "sides" of the thin central semiconductor region which extend up from the substrate. Further, as noted in a prior submission of the applicants, incorporated herein by reference, Sano fails to provide for removal of the thin central semiconductor region. Claims 1 and 24 have been amended to clarify these aspects of the invention, thereby distinguishing Sano.

The Neudeck reference is more closely related to the present invention, because it concerns fabrication of a dual-gated SOI FET. However, Neudeck is a 1993 patent reflecting prior art technology which is concerned with a channel thickness of 0.1 μm (col 4, line 45), significantly larger than the scale of the channels

Received from < > at 8/18/03 11:48:42 PM [Eastern Daylight Time]

in the present invention. It would be surprising if Neudeck disclosed the techniques required by the present invention, and upon careful examination it is clear that Neudeck makes no such disclosure. Even a casual reading of Neudeck (col 5, line 1 to col 8, line 49; Figs. 1A-1H, 2A-2D, 3A-3J) discloses that the fabrication method of Neudeck bears very little relation to that of the present invention. It should be noted that in Neudeck the fabrication of the channel – which figures prominently in the present invention, in order to achieve "much tighter tolerances on channel thickness" (page 6, lines 21-22) – is observed but not focused on. The main focus of Neudeck is the independently controllable and self-aligned gates (col 3, lines 19-49). Claim 14 has been amended to clarify these distinctions between the present invention and Neudeck.

Having thus clarified the independent claims 1, 14 and 24, which are now believed to have been placed in proper condition for allowance, the rejections of the remaining claims, which are dependent thereon, are similarly overcome.

In view of the foregoing, it is requested that the application be reconsidered, that claims 1 and 14-30 be allowed, and that the application be passed to issue.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at 703-787-9400 (fax: 703-787-7557; email: clyde@wcc-ip.com) to discuss any other changes deemed necessary in a telephonic or personal interview.

Received from < > at 8/18/03 11:48:42 PM [Eastern Daylight Time]

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account 09-0456 (IBM-Burlington).

Respectfully submitted,

OFFICIAL

Clyde R Christofferson
Reg. No. 34,138

Whitham, Curtis & Christofferson, P.C.
11491 Sunset Hills Road, Suite 340
Reston, VA 20190
703-787-9400
703-787-7557 (fax)

Customer No. 30743

FAX RECEIVED
AUG 19 2003
GROUP 2800

FAX RECEIVED
AUG 19 2003
GROUP 2800